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AMENDMENTS TO THE CLAIMS

Claims 1-15 are currently pending.

1. (Previously presented)A process of fabricating conductive structures in features of an insulator layer on a substrate comprising:

applying a layer of conductive material over the insulator layer so that the layer of conductive material covers field regions adjacent the features and fills in the features;

annealing the layer of conductive material to establish a grain size differential between the conductive material which covers the field regions and the conductive material which fills in the features by forming small grains in the conductive material covering the field regions and large grains in the conductive material over and filling the features, and

removing the conductive material with small grains faster than the conductive material with large grains.

2. (Previously presented)The process according to claim 1, wherein the layer of conductive material is applied so as to define a first layer thickness over the field regions and a second layer thickness in and over the features.

3. (Previously presented)The process according to claim 2, wherein the first layer thickness and the second layer thickness are dimensioned such that $d_1 \leq 0.5d_2$, with d_1 being the first layer thickness and d_2 being the second layer thickness.

4. (Previously presented)The process according to claim 3, wherein the first and the second layer thicknesses are dimensioned such that $d_1 \leq 0.3d_2$.

5. (Previously presented)The process according to claim 2, wherein applying the layer of conductive material over the insulator layer includes depositing the layer of conductive material over the insulator layer, and partially removing the layer of conductive material from over the field regions to establish a desired thickness differential between the first and second layer thicknesses.

6. (Previously presented)The process according to claim 2, wherein applying the layer of conductive material over the insulator layer includes depositing a planarized layer of conductive material over the insulator layer to establish a desired thickness differential between said first and second layer thicknesses.

7. (Previously presented)The process according to claim 5, wherein the first layer thickness and the second layer thickness are dimensioned such that $d_1 \leq 0.5d_2$, with d_1 being the first layer thickness and d_2 being the second layer thickness.

8. (Previously presented)The process according to claim 7, wherein the first and the second layer thicknesses are dimensioned such that $d_1 \leq 0.3d_2$.

9. (Previously presented)The process according to claim 6, wherein the first layer thickness and the second layer thickness are dimensioned such that $d_1 \leq 0.5d_2$, with d_1 being the first layer thickness and d_2 being the second layer thickness.

10. (Previously presented)The process according to claim 9, wherein the first and the second layer thicknesses are dimensioned such that $d_1 \leq 0.3d_2$.

11. (Previously presented)The process according to claim 1, wherein the conductive material is copper.

12. (Previously presented)The process according to claim 1, wherein the conductive material is a copper alloy.

13. (Original) The process according to claim 1, wherein removing the excess conductive material is done by chemical mechanical polishing, chemical etching, electrochemical etching, or any combination of chemical mechanical polishing, chemical etching and electrochemical etching.

14. (Previously presented)The process according to claim 1, wherein establishing the grain size differential also establishes a differential in chemical removal rates, physical removal rates, or both chemical and physical removal rates at which the excess conductive material can be removed from over the field regions and over the features.

15. (New) The process according to claim 1, where removing comprised chemical mechanical polishing having a chemical component dominant over a physical component.